

Engineering the Complex SOC: Fast, Flexible Design with Configurable Processors

By Chris Rowen

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Engineering the Complex SOC
The first unified hardware/software guide to processor-centric SOC design
Processor-centric approaches enable SOC designers to complete far larger projects in far less time. Engineering the Complex SOCis a comprehensive, example-driven guide to creating designs with configurable, extensible processors. Drawing upon Tensilica’s Xtensa architecture and TIE language, Dr. Chris Rowen systematically illuminates the issues, opportunities, and challenges of processor-centric design.
Rowen introduces a radically new design methodology, then covers its essential techniques: processor configuration, extension, hardware/software co-generation, multiple processor partitioning/communication, and more. Coverage includes:

- Why extensible processors are necessary: shortcomings of current design methods
- Comparing extensible processors to traditional processors and hardwired logic
- Extensible processor architecture and mechanisms of processor extensibility
- Latency, throughput, coordination of parallel functions, hardware interconnect options, management of design complexity, and other issues
- Multiple-processor SOC architecture for embedded systems
- Task design from the viewpoints of software andhardware developers
- Advanced techniques: implementing complex state machines, task-to-task synchronization, power optimization, and more
- Toward a “sea of processors”: Long-term trends in SOC design and semiconductor technology

For all architects, hardware engineers, software designers, and SOC program managers involved with complex SOC design; and for all managers investing in SOC designs, platforms, processors, or expertise.
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Editorial Review

From the Back Cover
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About the Author

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DR. CHRIS ROWEN is President, CEO, and Founder of Tensilica, a leader in the automatic generation of application-specific microprocessors for high-volume systems. He pioneered RISC architecture at Stanford, helped start MIPS Computer Systems, and served as VP/General Manager of the Design Reuse Group at Synopsys. He holds a Ph.D. in electrical engineering from Stanford.

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This book is aimed at the architects, designers, and programmers involved with complex SOC design. Managers of companies making significant investments in SOC designs and platforms will also find the essential changes in design process and architecture of platform hardware and software important to understand. These changes may directly or indirectly influence investment strategies, core competencies, and organization structure over time.

The book outlines the major forces changing the SOC design process and introduces the concept of SOC design using extensible processors as a basic design fabric. It teaches the essentials of extensible processor architecture, tools for instruction-set extension, and multiple-processor SOC architecture for embedded systems. It uses examples from Tensilica's Xtensa architecture and the Tensilica Instruction Extension (TIE) language throughout to give a precise, practical, and up-to-date picture of the real issues and opportunities associated with this new design method. You will find enough information on Xtensa and TIE to understand the methodology, though this book does not attempt to serve as comprehensive product documentation for either.

This book does not offer equal emphasis to all methodologies. Instead, it concentrates on the proposed benefits of this new SOC design methodology, highlighting the opportunities and dealing with issues associated with conversion from a gate-centric to a processor-centric SOC design methodology.

The first part of this book provides a high-level introduction to the many SOC design problems and their solutions. The middle sections give a more detailed look at how extensible processors compare to both traditional processors and hardwired logic. It also discusses how the essential mechanisms of processor extensibility address both the computation and communications needs of advanced SOC architectures. The later sections give a series of detailed examples to reinforce the applicability of the new SOC design method.

This introduction exposes the basic issues in SOC design and the motivation for considering an overhaul of the hardware and software structures and methods used for SOC development.

Chapter 2 provides a current view of SOC hardware structure, software organization, and chip-development flow. This chapter exposes the six basic shortcomings of the current SOC design method and explains why new structures and processes are necessary.

Chapter 3 introduces the new SOC design approach based on use of extensible processors across all control and data-processing functions on the chip. It briefly discusses how this approach addresses the six big problems.

Chapter 4 takes a top-down approach to processor-centric SOC architecture, looking at overall data flow through complex system architectures. The chapter shows how complex functions are decomposed into function blocks which may often be implemented as application-speci fic processors. Key issues include latency and throughput of blocks, programming models for coordination of parallel functions, hardware interconnect options, and management of complexity across the entire chip design.

Chapters 5 and 6 dig down into the design of the individual tasks. Chapter 5 looks at task design through the eyes of the software developer, especially the process of taking a task originally intended to run on a general-purpose processor and running that task on an applicationspeci fic processor. The chapter shows how application-specific processors fit the use model of traditional embedded processor cores while adding simple mechanisms that dramatically improve the performance and efficiency of complex tasks. This chapter includes a simple introduction to the principles of the Xtensa architecture, including Flexible Length Instruction Extensions (FLIX) and fully automated instruction-set generation.

Chapter 6, by contrast, looks at task design through the eyes of the hardware developer, especially at the process of taking a hardware function and translating it into an application-speci fic processor with comparable performance but thorough programmability. The chapter establishes the basic correspondence between hardware pipelines and processor pipelines and recommends techniques for efficient mapping of traditional hardware functions (including highbandwidth, low-latency functions) into application-specific processors.

Chapter 7 deals with a series of more advanced SOC-design topics and issues, including techniques for implementing complex state machines, options for task-to-task communication and synchronization, interfaces between processors and remaining hardware blocks, power optimization, and details of the TIE language.

Chapter 8, the final chapter, looks down the road at the long-term future of SOC design, examining basic trends in design methodology and semiconductor technology. It paints a 10 to 15 year outlook for the qualitative and quantitative changes in design, in applications, and in the structure of the electronics industry.

The book uses a number of related terms in the discussion of SOC design. An SOC design methodology is the combination of building blocks, design generators, architectural guidelines, tools, simulation methods, and analysis techniques that together form a consistent environment for development of chip designs and corresponding software. The book generally refers to the recommended method as the advanced SOC design or processor-centric SOC design methodology. Occasionally, we use the phrase MPSOC design methodology for multiple-processor system- on-chip design methodology to emphasize the role of processors, often combined in large numbers, as the basic building blocks for flexible SOCs. The ultimate vision is a role for configurable processors so common, so automatic, and so pervasive that we can rightly call the result a ‘sea of processors.’ Within a decade, processors could become the new logic gate, with hundreds or thousands of processors per chip and application-specific configuration of processors as routine as logic synthesis is today.

This book touches on a range of hardware, software, and system-design issues, but it cannot hope to cover each of these topics comprehensively. Rather than interrupt the flow with extensive footnotes and technical references, each chapter ends with a section for further reading. These sections highlight significant technical papers in the domain covered by each chapter and list additional books that may augment your understanding of the subject.

This book uses Tensilica’s Xtensa processor architecture and tools to illustrate important ideas. This book does not attempt, however, to fully document Tensilica’s products. Contact Tensilica for more complete details at http://www.tensilica.com. Other approaches to automatic processor generation are mentioned in the book, especially in Chapter 3.

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